CLAIMS

What is claimed is:

1. A memory cell comprising:

a first PMOS transistor;

a first NMOS transistor coupled to the first PMOS transistor;

a second PMOS transistor; and

a second NMOS transistor coupled to the second PMOS transistor;

the first and second PMOS transistors receiving a bias control signal.

2. The memory cell of claim 1 further comprising:

a first storage node coupled between the first PMOS transistor and the first NMOS transistor; and

a second storage node coupled between the second PMOS transistor and the second NMOS transistor.

3. The memory cell of claim 2 wherein the bias control signal delivers a forward bias voltage to the first and second PMOS transistors whenever the memory cell is operating in a standby mode.

4. The memory cell of claim 3 wherein the forward bias voltage enables the first storage node to maintain a storage value by providing an off-state leakage current from the first PMOS transistor.

5. The memory cell of claim 2 wherein the bias control signal delivers a reverse bias voltage to the first and second PMOS transistors whenever the memory cell is operating in a read mode.

6. The memory cell of claim 5 wherein the reverse bias voltage prevents the memory cell from switching its value during the read mode.

7. A memory device comprising:

an N-well;

a plurality of memory cells, each memory cell including:

a P-channel component; and

a N-channel component, the P-channel component being formed within the N-well;

a gap cell formed within the N-well; and

a contact within the gap cell that provides a bias control signal to each of the P-channel components within a memory cell.

8. The memory device of claim 7 wherein the P-channel component of each memory cell comprises:

a first PMOS transistor; and

a second PMOS transistor, the first and second PMOS transistors receiving a bias control signal.

9. The memory device of claim 8 wherein the N-channel component of each memory cell comprises:

a first NMOS transistor coupled to the first PMOS transistor; and

a second NMOS transistor coupled to the second PMOS transistor;

10. The memory device of claim 9 further comprising:

a first storage node coupled between the first PMOS transistor and the first NMOS transistor; and

a second storage node coupled between the second PMOS transistor and

the second NMOS transistor.

11. The memory device of claim 10 wherein the bias control signal delivers a forward bias voltage to the first and second PMOS transistors whenever the memory cell is operating in a standby mode.

12. The memory device of claim 11 wherein the forward bias voltage enables the first storage node to maintain a storage value by providing an off-state leakage current from the first PMOS transistor.

13. The memory device of claim 10 wherein the bias control signal delivers a reverse bias voltage to the first and second PMOS transistors whenever the memory cell is operating in a read mode.

14. The memory device of claim 13 wherein the reverse bias voltage prevents the memory cell from switching its value during the read mode.

15. A computer system comprising:

a microprocessor; and

a cache memory device, the cache memory device including:

a plurality of memory cells, each memory cell including a P-channel component and a N-channel component, the P-channel component formed within the N-well;

a gap cell formed within the N-well; and

a contact within the gap cell that provides a bias control signal to each of the P-channel components within a memory cell.

16. The computer system of claim 15 wherein the P-channel component of each memory cell comprises:

a first PMOS transistor; and

a second PMOS transistor, the first and second PMOS transistors receiving a bias control signal.

17. The computer system of claim 16 wherein the N-channel component of each memory cell comprises:

a first NMOS transistor coupled to the first PMOS transistor; and

a second NMOS transistor coupled to the second PMOS transistor;

18. The computer system of claim 17 further comprising:

a first storage node coupled between the first PMOS transistor and the first NMOS transistor; and

a second storage node coupled between the second PMOS transistor and the second NMOS transistor.

19. The computer system of claim 18 wherein the bias control signal delivers a forward bias voltage to the first and second PMOS transistors whenever the memory cell is operating in a standby mode.

20. The computer system of claim 19 wherein the forward bias voltage enables the first storage node to maintain a storage value by providing an off-state leakage current from the first PMOS transistor.

21. The computer system of claim 18 wherein the bias control signal delivers a reverse bias voltage to the first and second PMOS transistors whenever the memory cell is operating in a read mode.

22. The computer system of claim 21 wherein the reverse bias voltage prevents the memory cell from switching its value during the read mode.

23. The computer system of claim 15 wherein the cache memory device is

coupled to the microprocessor.

24. The computer system of claim 15 wherein the cache memory device is included within the microprocessor.